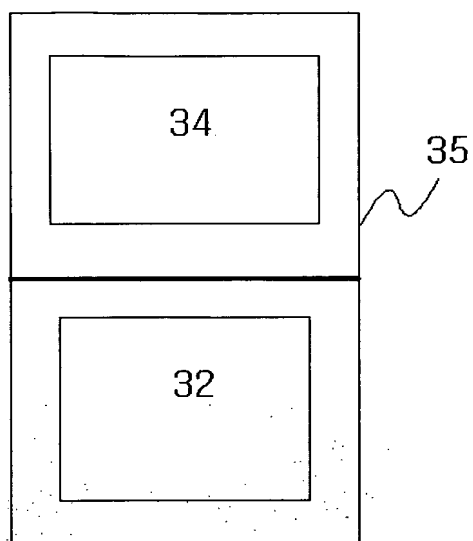
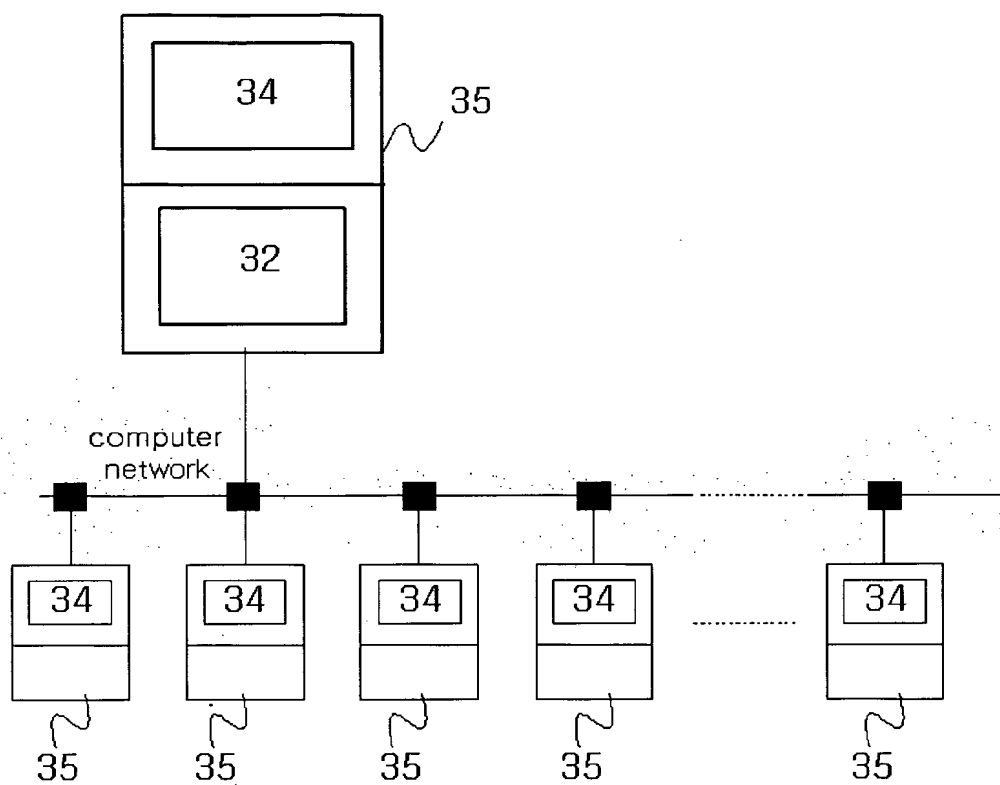


[FIG. 1]

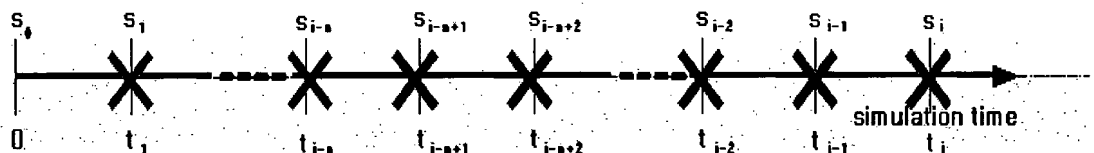


[FIG. 2]



[FIG. 3]

i) 1st simulation



X simulation state saving points, or DUV design state saving points, and TB state saving points, if necessary

ii) Post-1st simulation

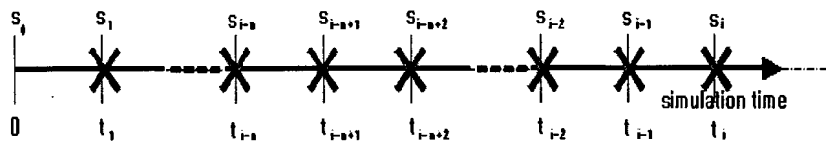


● simulation state re-storing points, or DUV design state re-storing points, and TB state storing points, if necessary

[FIG. 4]

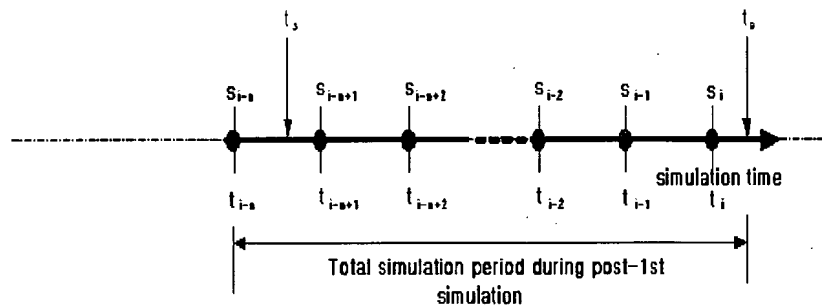
i) 1st simulation

X simulation state saving points, or DUV design state saving points, and TB state saving points, if necessary

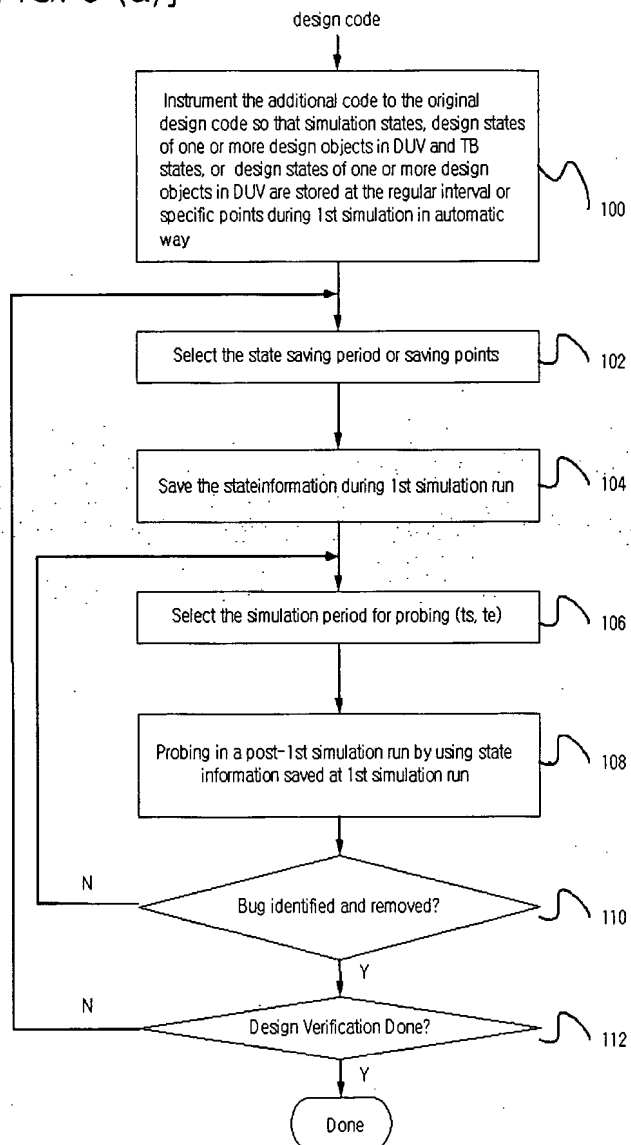


ii) Post-1st simulation

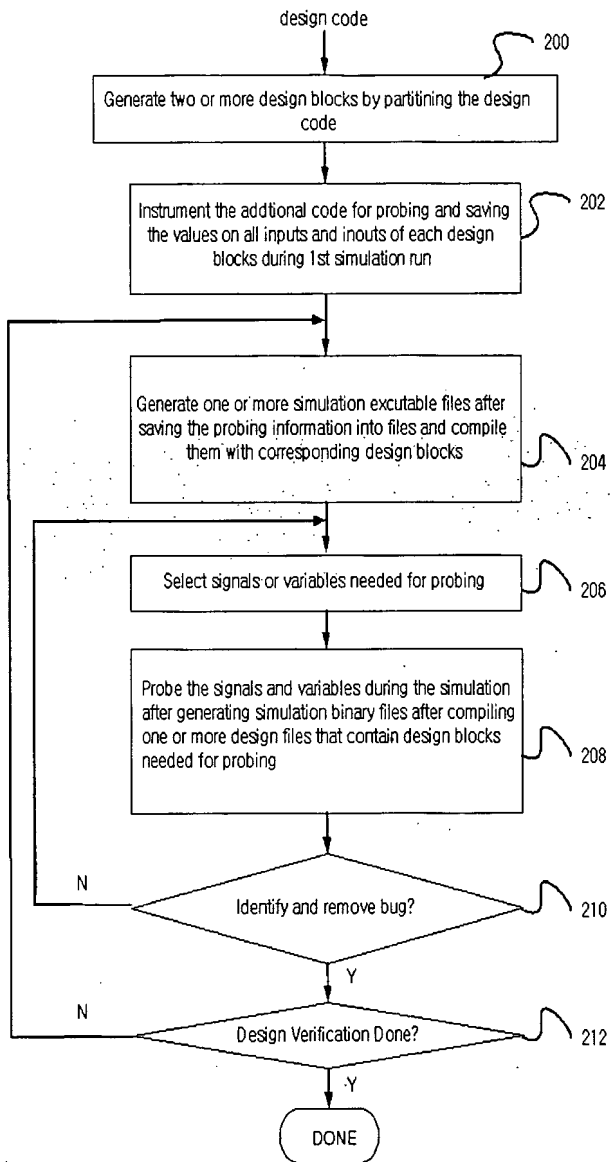
● simulation state re-storing points, or DUV design state re-storing points, and TB state re-storing points, if necessary



[FIG. 5 (a)]

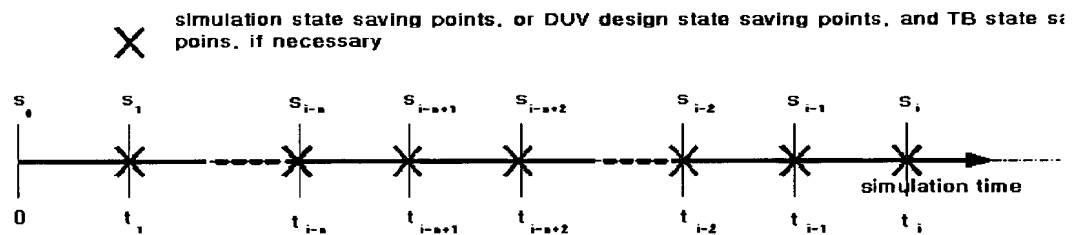


[FIG. 5 (b)]

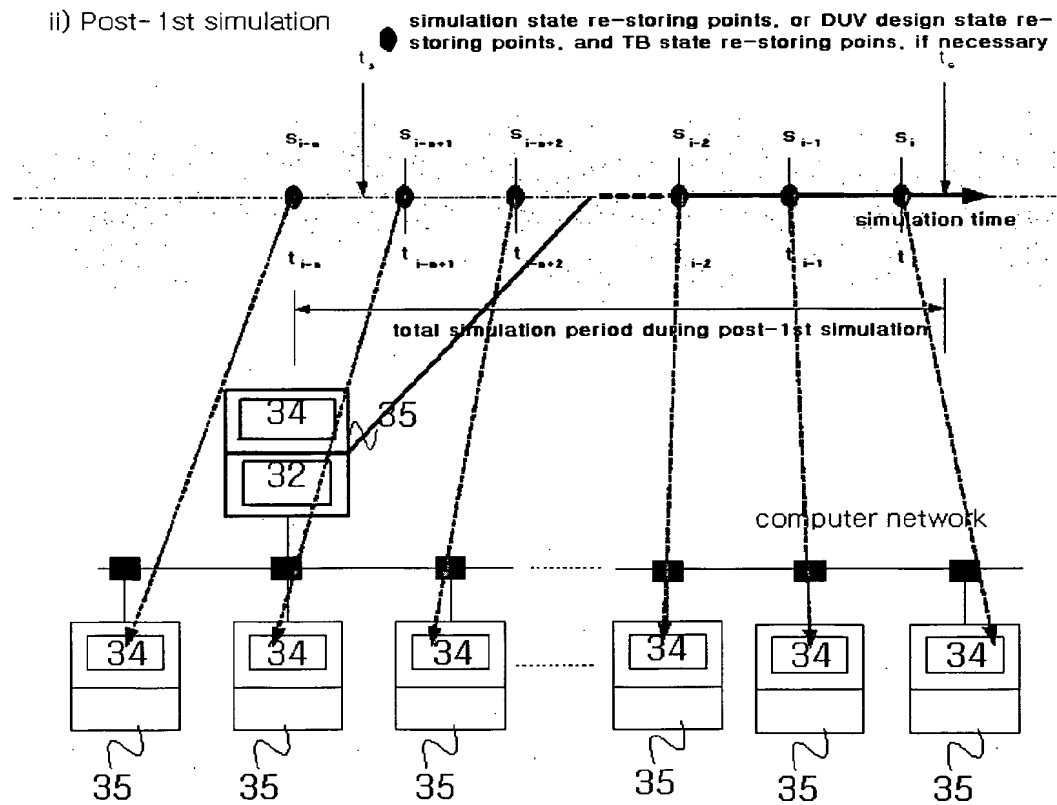


[FIG. 6 (a)]

i) 1st simulation

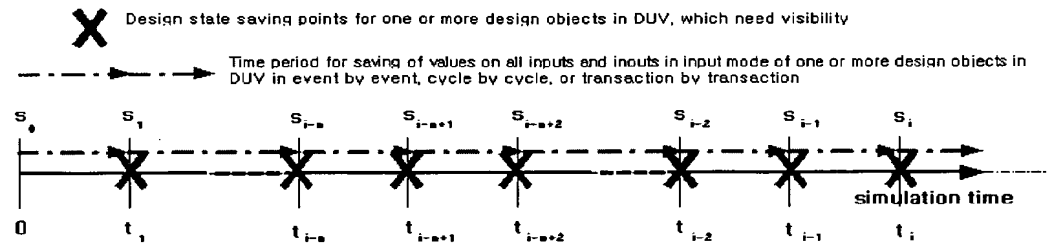


ii) Post-1st simulation

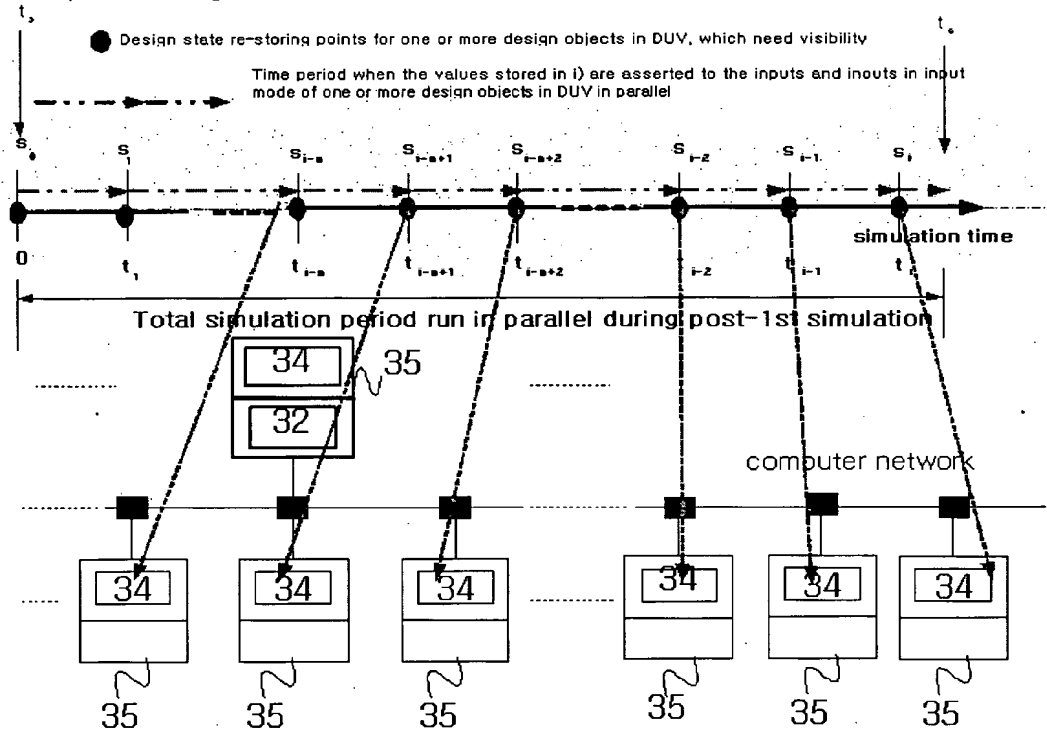


[FIG. 6 (b)]

i) 1st RTL simulation

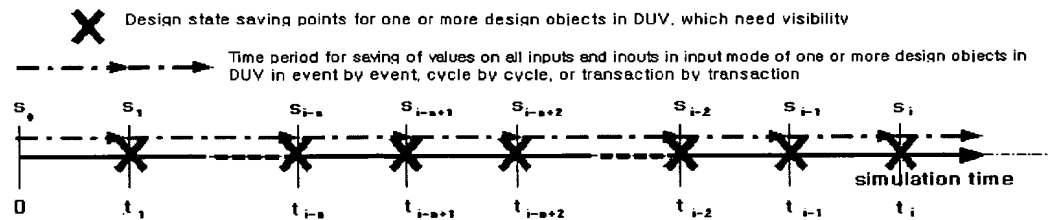


ii) Post-1st gate-level simulation

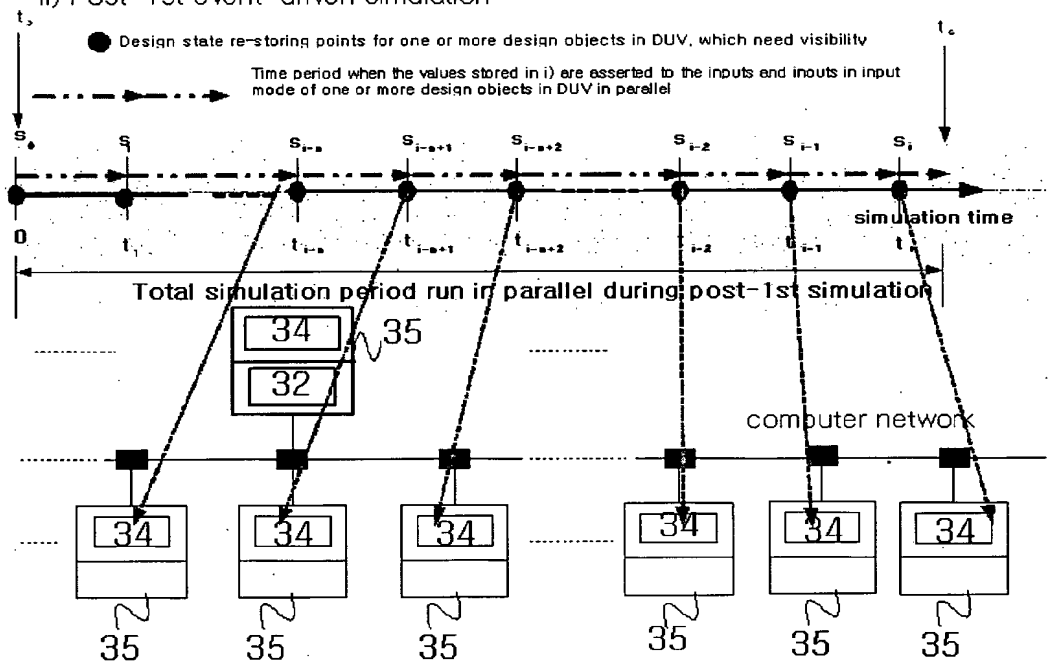


[FIG. 6 (c)]

i) 1st cycle-based simulation



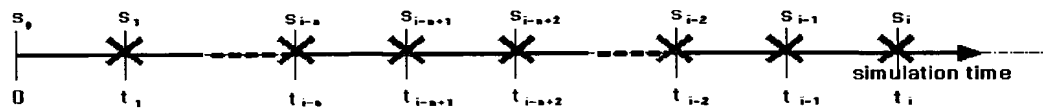
ii) Post-1st event-driven simulation



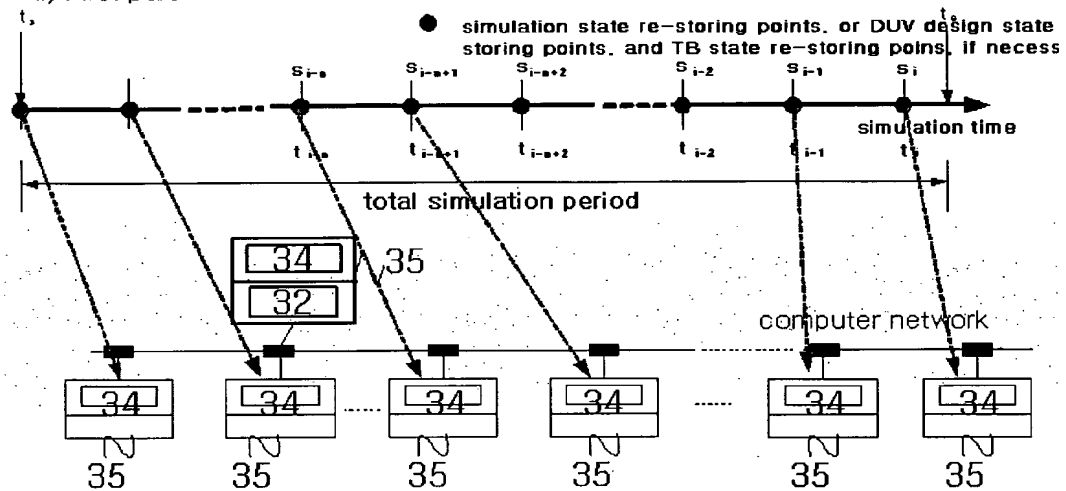
[도 6 (d)]

i) 1st simulation

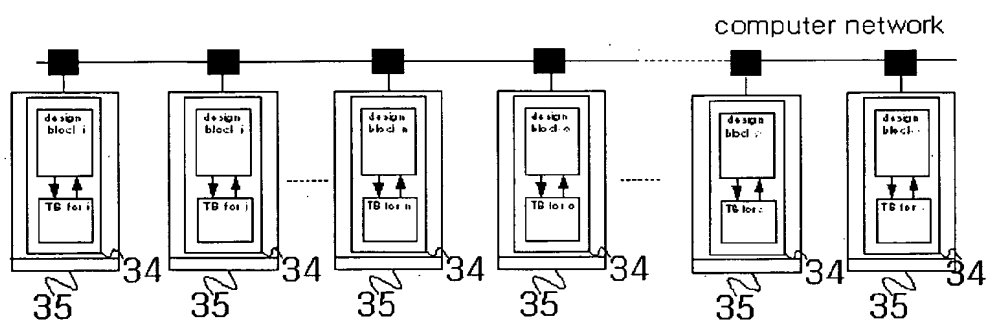
× simulation state saving points, or DUV design state saving points, and TB state saving points, if necessary



ii) First parallel simulation after 1st simulation

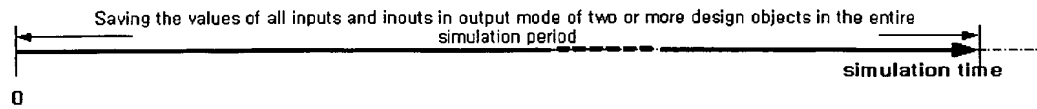


iii) Second parallel simulation after 1st simulation

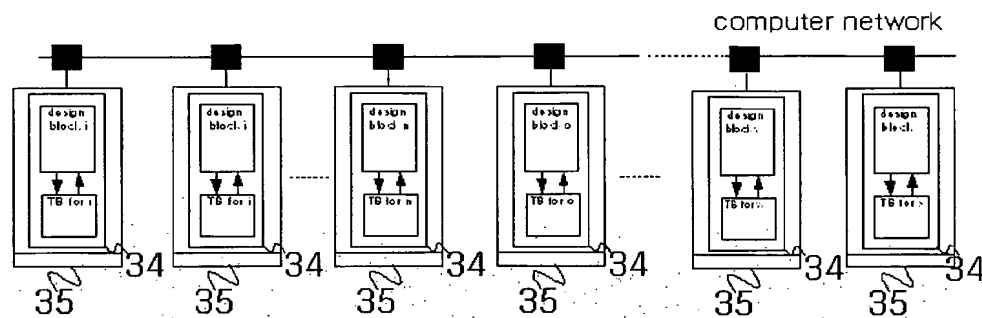


[FIG. 6 (e)]

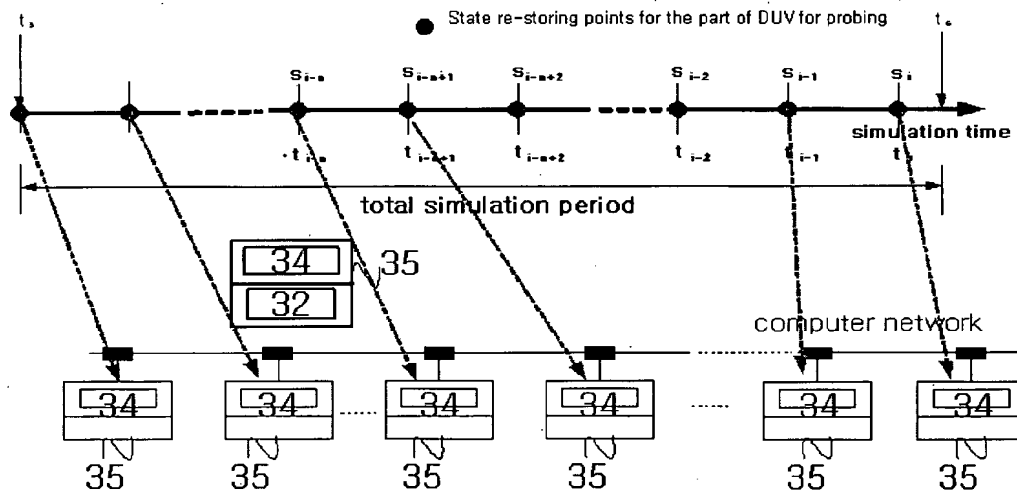
i) 1st simulation



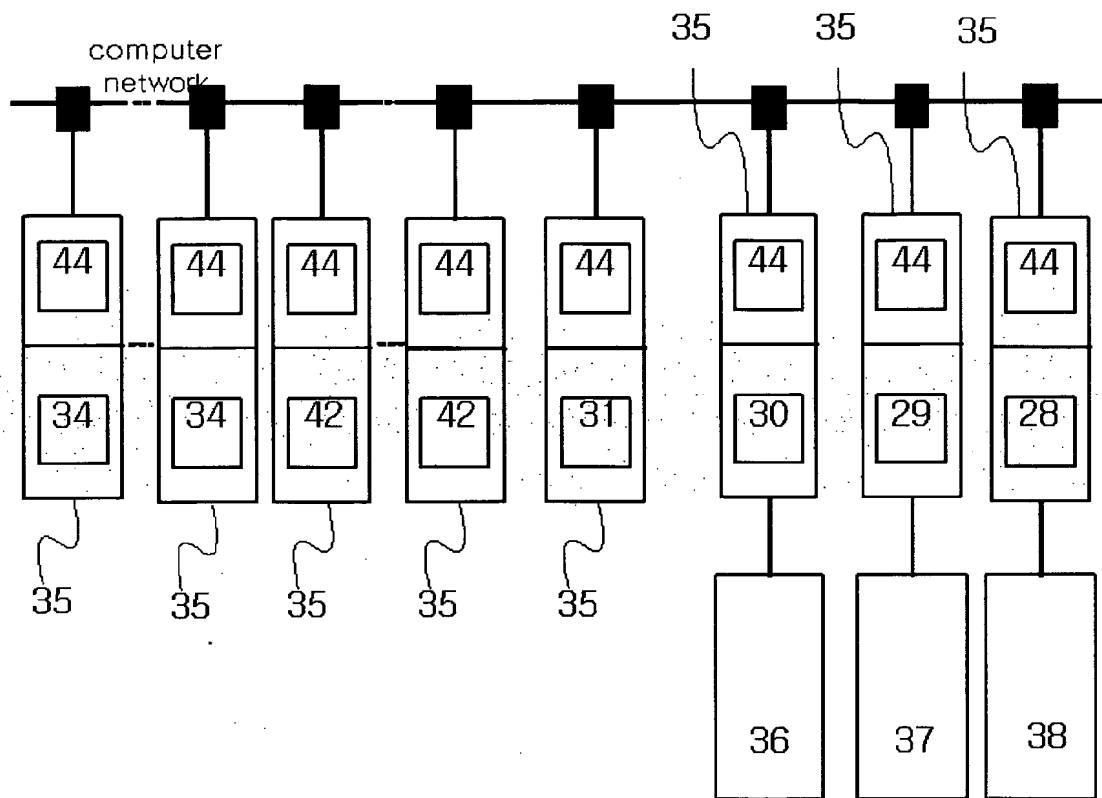
ii) 1st parallel simulation after 1st simulation



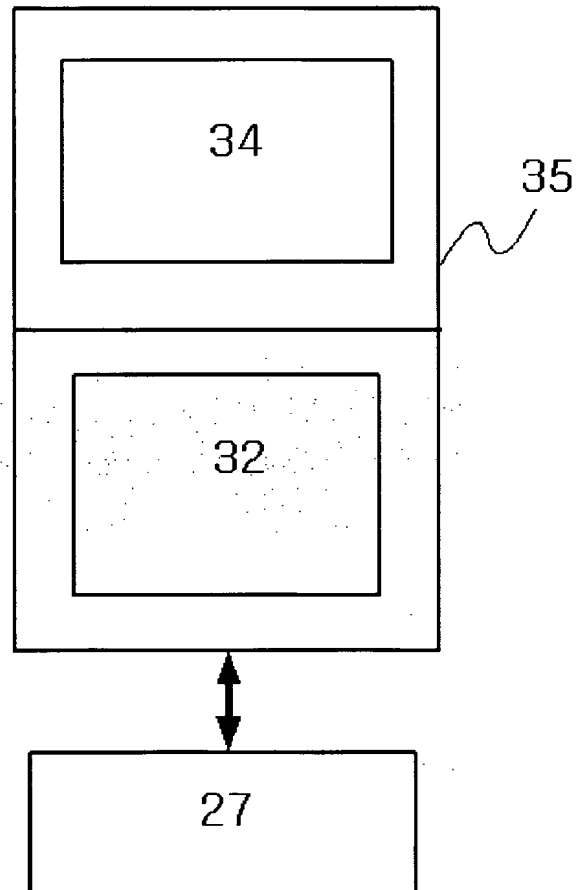
iii) 2nd parallel simulation after 1st simulation



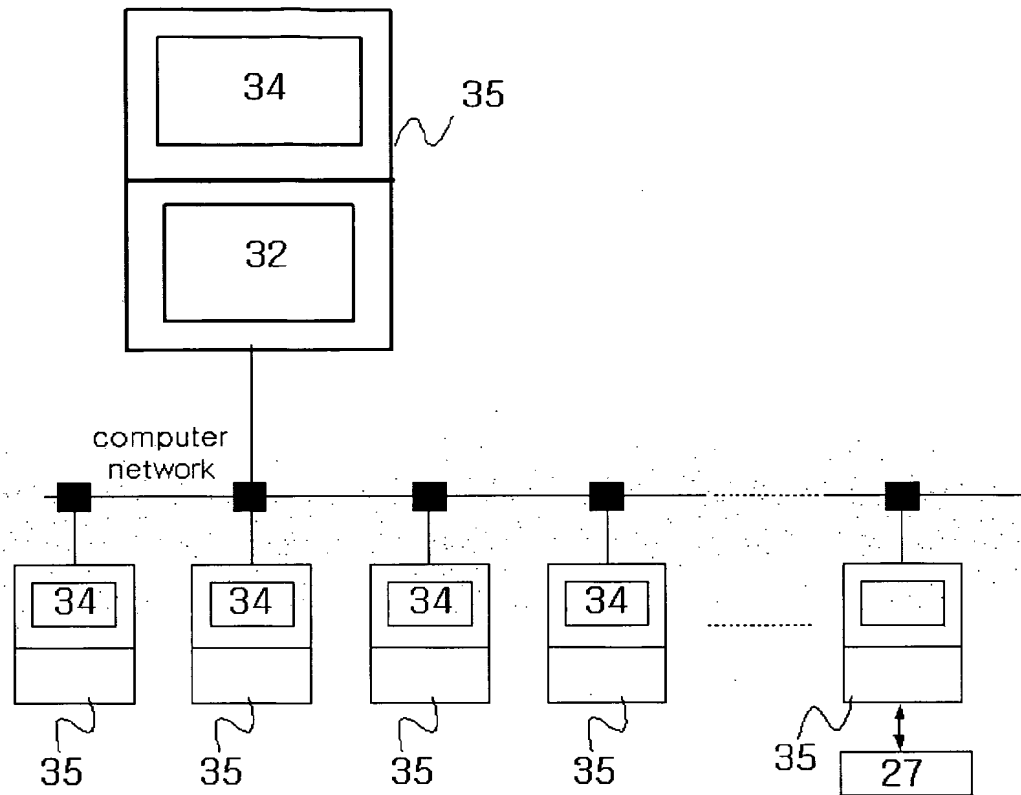
[FIG. 7]



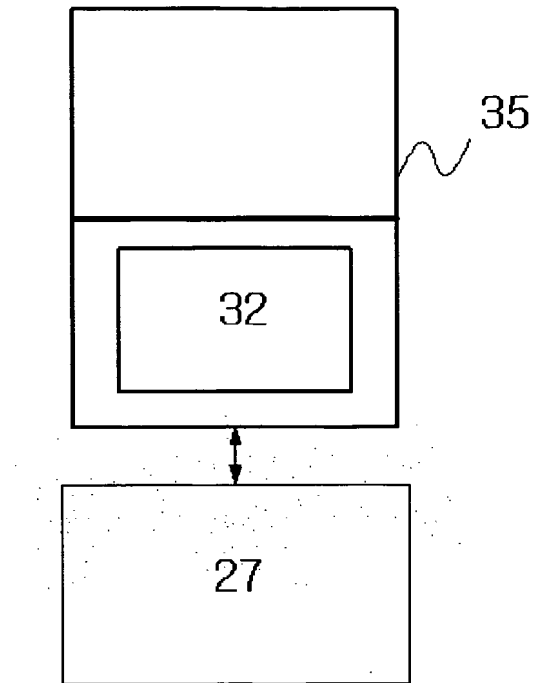
[FIG 8]



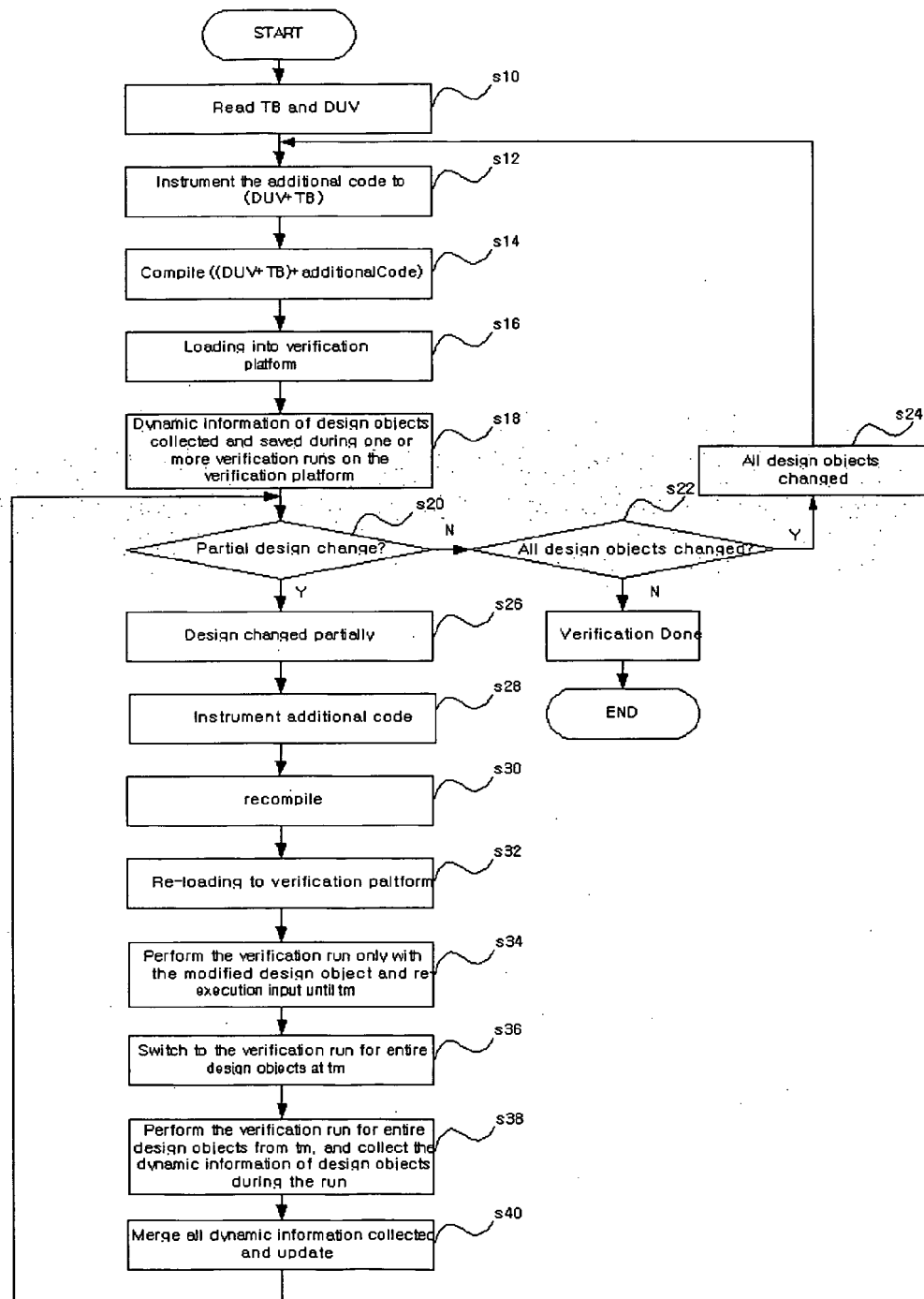
[FIG. 9]



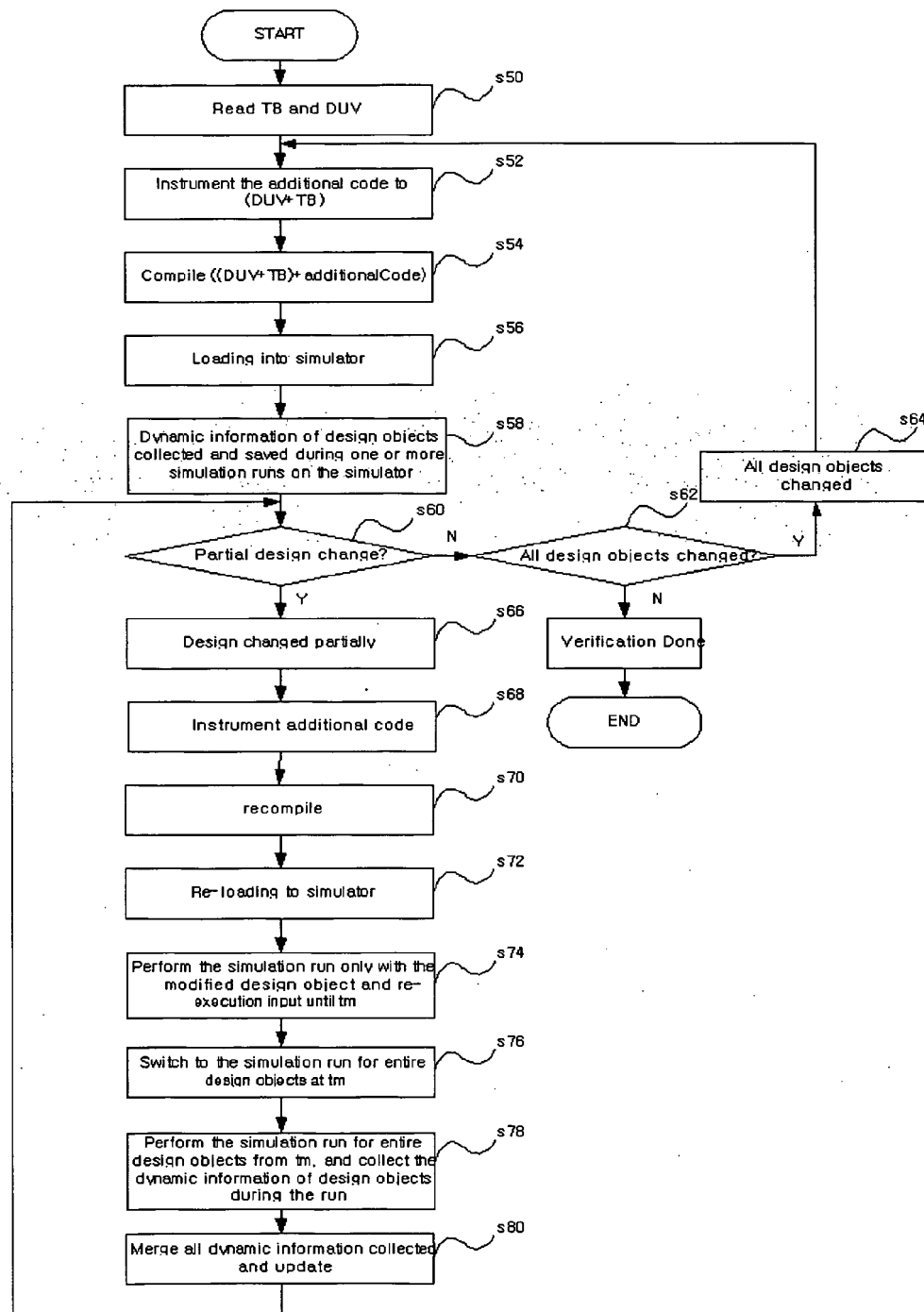
[FIG. 10]

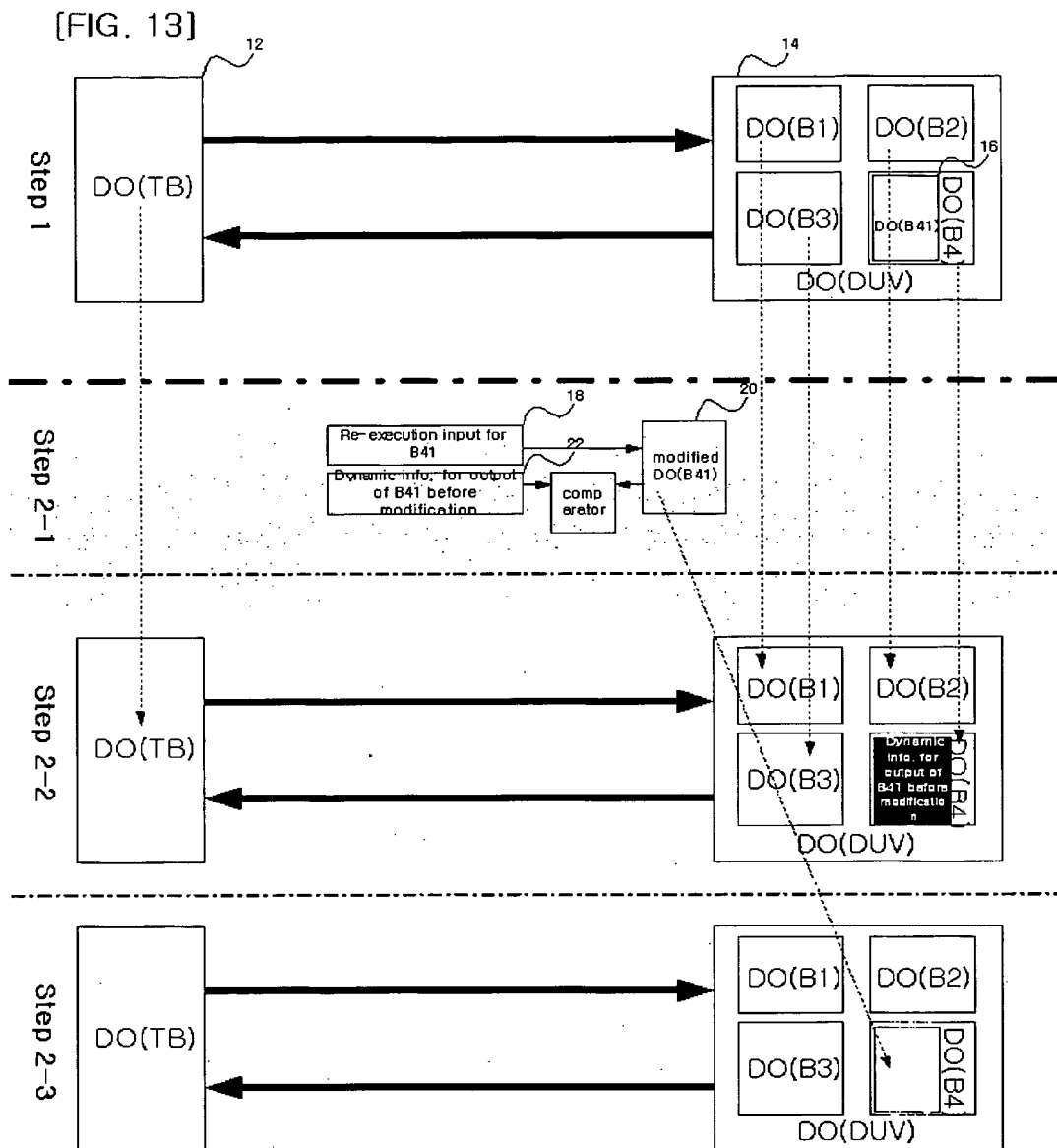


[FIG. 11]

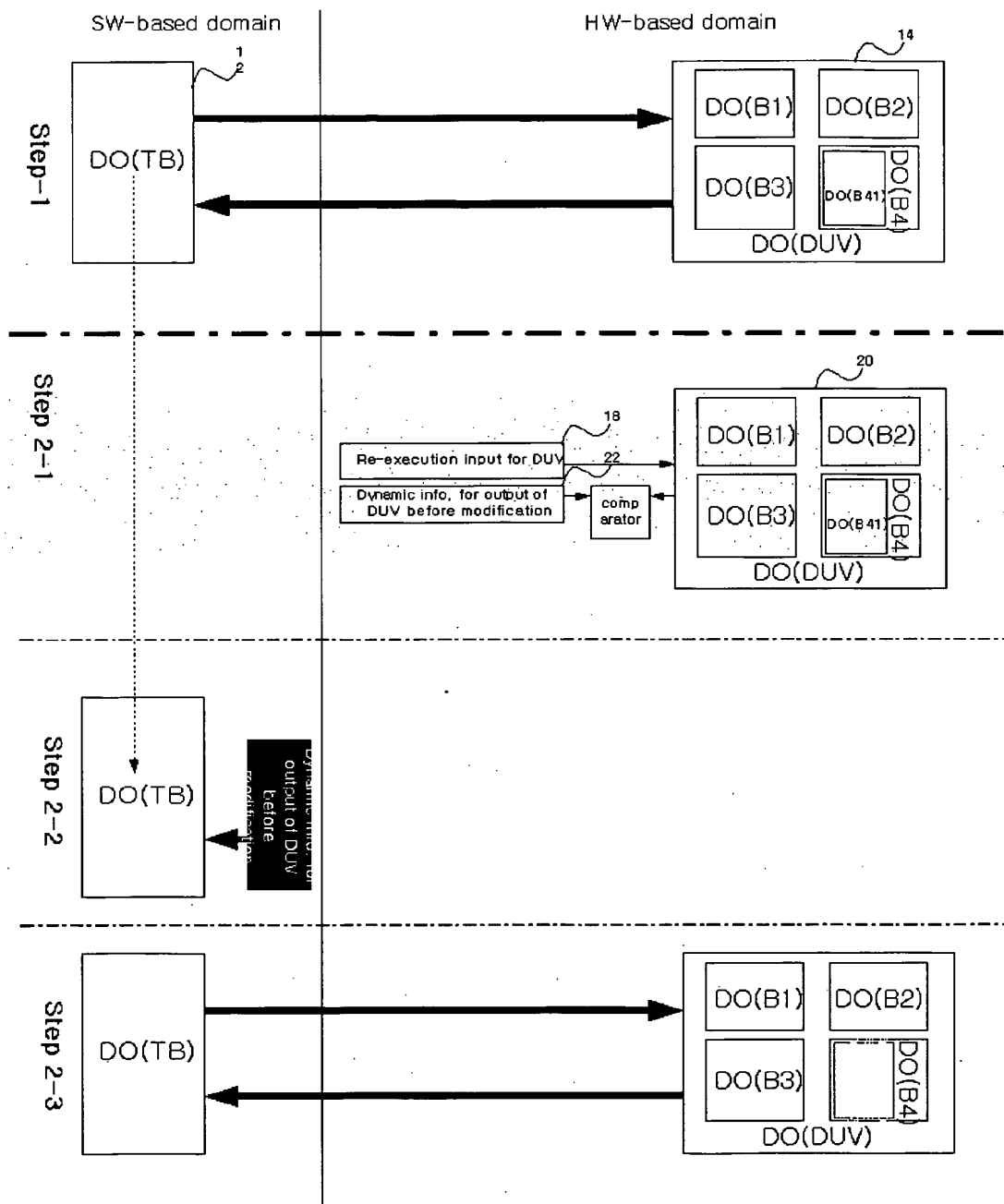


[FIG. 12]





[FIG. 14]



[FIG. 15]

